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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|------------------------|-------------|----------------------|---------------------|------------------|
| 10/079,235 | 02/19/2002 | Robert O. Conn | X-736 US | 7201 |
| 24309 | 7590 | 05/10/2004 | EXAMINER | |
| XILINX, INC | | | HU, SHOUXIANG | |
| ATTN: LEGAL DEPARTMENT | | | | |
| 2100 LOGIC DR | | | ART UNIT | PAPER NUMBER |
| SAN JOSE, CA 95124 | | | 2811 | |

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|--------------------------|------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/079,235 | CONN, ROBERT O. | |
| | Examiner Shouxiang Hu | Art Unit 2811 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 09 February 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 2-51 is/are pending in the application.
- 4a) Of the above claim(s) 14-16, 26-51 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 2-13 and 17-25 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

In view of the previous Office action, claims 2-51 are pending in this application; and claims 2-13 and 17-25 remain active in this office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-13 and 17-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masushige et al. ("Masushige"; JP 4-226039, August 14, 1992) in view of Vu et al. ("Vu"; US 5,256,562).

Masushige discloses a method (see Figs. 1-3; also see its English abstract) for altering the semiconductor characteristics of a semiconductor element (FET) formed on a substrate (1), comprising the step of directing an energy beam (6, a laser beam) at a first portion (including the channel region) of the semiconductor element through the backside of the substrate, wherein the energy beam is substantially absorbed by the first portion.

Although Masushige does not expressly discloses that the method can further comprises the step of thinning the substrate, Vu teaches a step of thinning the substrate

having a FET thereon by bonding it on supporting substrate for forming the pixel electrode on the back surface to better activate the liquid crystal layer (see col. 9, lines 47-55; also see the supporting substrate 110' and the thinned substrate 34' in Figs. 7D-7H).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Vu's step of thinning the substrate into the method of Masushige, so that a TFT display device with better activation for the liquid crystal layer would be obtained.

Regarding claims 2-5, it is noted that it is art-known that a powerful energy beam can be generated from a CO₂ laser, a YAG laser, or a laser from a photomask-repairing laser ablation system, as evidenced in the prior references such as Freedenberg et al. (US 5,609,780; see col. 1, lines 10-15, and col. 4, lines 60-65); and/or Hashimoto et al. (US 5,318,869; see the abstract). Regarding claim 4, it is further noted that lights with the recited wavelength can be naturally generated from a CO₂ laser.

Regarding claims 7 and 10, the FET in Vu further includes a passivation layer (36) thereon, along with an adhesive layer (82').

Regarding claims 8 and 9, it is art-known that an oxide layer can be formed on the support structure in order to form better bonding through naturally covalently bonding between the oxide layer and a passivation layer covering the starting substrate, as evidenced in the prior art references such as Nakasato et al. (US 5,071,785; see the passivation layer 1c covering the starting substrate 1b and the oxide layer covering the supporting substrate 1a in Figs. 4A-4C.

Regarding claims 11-13, it is noted that grinding, CMP and etch each are art-known methods for thinning a substrate.

Regarding claims 17, 18 and 21, it is noted that silicon wafer, GaAs wafer and a substrate comprising an amorphous silicon layer each are art-known starting substrate or layer for forming semiconductor elements thereon.

Regarding claim 19, the substrate of Masushige further comprises an insulating plate (1 and/or 2).

Regarding claims 21-25, the semiconductor element in Masushige further comprises: source/drain regions (9, 10); gate insulator (4, commonly formed of an oxide); a channel region (11); and a gate (5). In addition, regarding claims 22-25, it is further noted that metal gate structure and salicide gate/source/drain structure each are art-known FET structures for better electrode conductance and/or alignment, as evidenced in the prior art references such as: Havemann (US 5,252,502; see the metal gate 42 in Figs. 1l, 2m and 3o); and Isobe et al. (US 6,337,594; see the TiSi salicide gate 6a, source 9a and drain 10a in the cover page figure).

Response to Arguments

2. Applicant's arguments filed on February 9, 2004 have been fully considered but they are not persuasive.

Applicant's main arguments include: Vu and Masushige are incompatible, as Vu requires an opaque shield.

In response, it is noted that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, both Vu and Masushige teach to form thin film transistors (TFT) with a crystallized channel-forming layer. Masushige discloses the claimed invention of a method, including the steps of altering the semiconductor characteristics of a TFT by directing an energy beam at the channel region through the backside of the substrate, except that Masushige does not expressly discloses that the method can further comprises the step of thinning the substrate. Vu is cited for shown that one of the ordinary skill in the art would readily recognize that in various art-known applications, such a substrate-thinning step is commonly desired for achieving better performance including better activation for the liquid crystal layer in the applications. In Masushige, the energy beam (6, a laser beam) is directed to the first portion (including the channel region) from the backside and through the whole thickness of the substrate; and the TFT is formed on the substrate with its whole thickness. In Vu, the TFT is also first formed on the substrate with its whole thickness; and the opaque shield (76') is formed after the substrate (30') has been thinned. Therefore, one of ordinary skill in the art would readily recognized that the thinning step of Vu can be readily incorporated into the method of Masushige to form a TFT device with the substrate therein being thinned after the step of directing the energy beam at the first portion, so as to make the TFT

device suitable to the art-known applications such as the one of Vu; and that, if desired, the opaque shield in Vu can always be readily formed after the substrate-thinning step in the method collectively taught above by Masuhige and Vu.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH

May 5, 2004



SHOUXIANG HU
PRIMARY EXAMINER